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(72) Inventors:  
• Alers, Glenn B.  
Chatham, New Jersey 07928 (US)  
• Roy, Pradip Kumar  
Orlando, Florida 32819 (US)

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(74) Representative:  
Watts, Christopher Malcolm Kelway, Dr. et al  
Lucent Technologies (UK) Ltd,  
5 Mornington Road  
Woodford Green Essex IG8 OTU (GB)

(71) Applicant:  
LUCENT TECHNOLOGIES INC.  
Murray Hill, New Jersey 07974-0636 (US)

(54) Method for making an integrated circuit capacitor including tantalum pentoxide

(57) A method for making an integrated circuit capacitor which in one embodiment preferably comprises the steps of: forming, adjacent a semiconductor substrate, a first metal electrode comprising a metal nitride surface portion; forming a tantalum pentoxide layer on the metal nitride surface portion while maintaining a temperature below an oxidizing temperature of the metal; remote plasma annealing the tantalum pentoxide layer; and forming a second electrode adjacent the tantalum pentoxide layer. The step of forming the tantalum pentoxide layer preferably comprises chemical vapor deposition of the tantalum pentoxide at a temperature below about 500°C. Accordingly, oxidation of the metal is avoided and a high quality tantalum pentoxide is produced. The metal of the first metal electrode may comprise at least one of titanium, tungsten, tantalum, and alloys thereof.

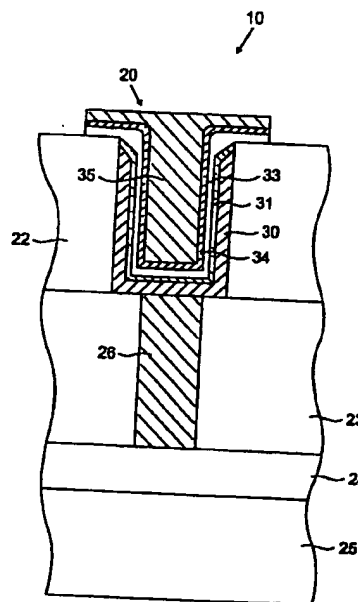


FIG. 1

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## Description

### Field Of The Invention

[0001] The present invention relates to the field of semiconductors, and, more particularly, to a method for making a capacitor in an integrated circuit.

### Background Of The Invention

[0002] An integrated circuit typically includes transistors and other devices formed on a semiconductor substrate. A capacitor may be provided as part of an integrated circuit by forming a first conductive electrode, a dielectric layer on the first electrode, and a second conductive electrode on the dielectric layer. Such capacitors are commonly used in memory cells for DRAM devices, for example, as well as in analog-to-digital converters and other circuits.

[0003] As disclosed in U.S. Patent No. 5,910,880 to DeBoer et al., for example, tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) is a desired material for a capacitor dielectric because of its relatively high dielectric constant of about 25. In comparison, silicon nitride has a dielectric constant of about 8, and silicon dioxide has a dielectric constant of about 4. The high dielectric constant of tantalum pentoxide allows a thinner layer of the material to be used between the electrodes to achieve the same capacitance as using other lower dielectric constant materials.

[0004] A typical construction of such a capacitor includes a first or lower electrode of polycrystalline silicon. A first barrier layer of silicon nitride is typically provided to protect the polycrystalline silicon from forming into silicon dioxide and to prevent diffusion as the tantalum pentoxide is deposited thereon. A second barrier layer of titanium nitride or tungsten nitride may be deposited over the tantalum pentoxide prior to forming the polycrystalline silicon or metal layer of the upper electrode.

[0005] U.S. Patent No. 5,622,888 to Sekine et al. discloses making a DRAM capacitor also using tantalum pentoxide. A layer of tungsten is sputter deposited on a polysilicon lower electrode. The tantalum pentoxide is deposited; by chemical vapor deposition (CVD) at a temperature in a range of 300 to 600°C. Unfortunately, the higher temperatures may have a tendency to oxidize the tungsten. Thereafter, the tantalum pentoxide is densified by a plasma using an oxygen gas at a temperature ranging from 200 to 600°C. An upper tungsten electrode is formed on the tantalum pentoxide.

[0006] Despite continuing development in the field of integrated circuit capacitors using tantalum pentoxide as the dielectric, there still exists a need to further develop the manufacturing process to produce such capacitors having relatively high capacitance values and other desirable properties.

## Summary Of The Invention

[0007] In view of the foregoing background, it is therefore an object of the invention to provide a method for making an integrated circuit capacitor having a relatively high capacitance.

[0008] This and other objects, features and advantages in accordance with the present invention are provided by a method for making an integrated circuit capacitor which in one embodiment preferably comprises the steps of: forming a first metal electrode adjacent a semiconductor substrate; forming a tantalum pentoxide layer on the first metal electrode while maintaining a temperature below an oxidizing temperature thereof; performing at least one remote plasma anneal of the tantalum pentoxide layer while also maintaining a temperature below the oxidizing temperature of the first metal electrode; and forming a second electrode adjacent the tantalum pentoxide layer while also maintaining a temperature below the oxidizing temperature of the first metal electrode. The step of forming the tantalum pentoxide layer preferably comprises chemical vapor deposition of the tantalum pentoxide at a temperature below about 500°C, and, more preferably, below about 400°C. The CVD forming of the tantalum pentoxide may preferably be performed in less than about 10 minutes. In addition, the pressure during CVD is typically greater than about 3 Torr, such as in a range of 3 to 15 Torr.

[0009] To reduce damage to the tantalum pentoxide layer, the step of annealing preferably comprises exposing the tantalum pentoxide layer to a first remote plasma of pure nitrogen and to a second remote plasma including nitrogen and oxygen. Accordingly, oxidation of the metal of the first electrode is avoided and a high quality tantalum pentoxide is produced by the method of the invention.

[0010] The metal of the first metal electrode may comprise at least one of titanium, tungsten, tantalum, platinum, iridium, ruthenium, and alloys thereof. More preferably, the first metal electrode comprises at least one of titanium, tungsten, tantalum, and alloys thereof. Most preferably the metal comprises titanium nitride.

[0011] The method may further include the steps of: forming at least one dielectric layer adjacent the semiconductor substrate, and forming an opening in the at least one dielectric layer. Accordingly, the step of forming the first metal electrode layer may comprise forming the first metal electrode layer to line the opening in the at least one dielectric layer.

[0012] The step of forming the first metal electrode may comprise the steps of forming a first metal layer and nitridizing an upper surface portion thereof according to one embodiment. The step of nitridizing may preferably include exposing the first metal layer to a nitrogen containing ambient while maintaining a temperature below the oxidizing temperature of the metal. Alternatively, the step of forming the first metal electrode may comprise depositing a first metal layer and depositing a

metal nitride layer thereon while preferably maintaining a temperature below the oxidizing temperature of the metal. The nitridized surface portion may further enhance resistance to oxidization of the underlying metal, especially for tungsten, for example.

#### **Brief Description Of The Drawings**

##### **[0013]**

FIG. 1 is a schematic cross-sectional view of the capacitor made in accordance with the method of the invention.

FIG. 2 is a flowchart for the method for making an integrated circuit capacitor in accordance with the present invention.

#### **Detailed Description Of The Preferred Embodiments**

**[0014]** The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. The dimensions of layers and regions may be exaggerated in the figures for greater clarity.

**[0015]** Referring to FIGS. 1 and 2, the method for making an integrated circuit 10 including a capacitor 20 is now described. The illustrated embodiment of the method includes, after the start (Block 40), forming an opening in a dielectric layer 22 (Block 40). The integrated circuit 10 also includes other dielectric layers 23, 24 formed on the semiconductor substrate 25, as well as the illustrated via 26 for connecting to the capacitor 20 as will be readily appreciated by those skilled in the art. The present invention is primarily directed to forming a capacitor 20 to be used in embedded DRAM applications where high-speed logic circuits, including their metallizations, have already been formed on the substrate as will be readily appreciated by those skilled in the art.

**[0016]** At Block 44, a first metal layer 30 is formed to line the opening in the dielectric layer 22. The first metal layer may preferably include titanium, tungsten, tantalum, and alloys thereof. The first metal layer 30 may be titanium nitride, tungsten, or tantalum nitride in some preferred embodiments. Titanium nitride and tantalum nitride are especially preferred materials. In other embodiments, the first metal layer 30 may include at least one of platinum, ruthenium, iridium, and alloys thereof. The first metal layer 30 is preferably formed by

conventional CVD deposition techniques as will be readily appreciated by those skilled in the art without requiring further discussion herein.

**[0017]** If the first metal layer comprises tungsten, for example, it may be desirable to nitridize an upper surface portion thereof to produce the illustrated metal nitride layer 31 (Block 46). The tungsten nitride surface portion/further resist oxidation of the underlying tungsten as will be appreciated by those skilled in the art.

This nitridized surface portion can be formed by any of a number of conventional techniques, such as using a plasma and/or exposing the surface to a nitrogen containing ambient, such as ammonia, in a furnace. In another embodiment, the metal nitride layer 31 may be formed by conventional deposition techniques, such as CVD. The metal nitride layer 31 may be deposited while preferably maintaining a temperature below the oxidizing temperature of the metal. In other embodiments, such as, for example, where the first metal layer 30 comprises titanium nitride or tantalum nitride, the nitride layer 31 is not needed.

**[0018]** At Block 48, the tantalum pentoxide layer 33 is formed to serve as the capacitor dielectric layer. Of course, tantalum pentoxide is highly desirable as a dielectric for a capacitor in view of its relatively high dielectric constant value as compared to other conventional dielectric materials using in semiconductor manufacturing. The tantalum pentoxide layer 33 may be formed by a CVD process wherein  $\text{Ta}(\text{OC}_2\text{H}_5)_5$  and oxygen are combined as will be readily appreciated by those skilled in the art.

**[0019]** In accordance with the present invention, the deposition temperature is maintained below an oxidizing temperature of the first metal electrode. More particularly, the temperature is desirably maintained below about 500°C, and, more preferably, below about 400°C. As will be readily appreciated by those skilled in the art, the time period for the CVD deposition of the tantalum pentoxide layer 33 is generally determined based upon the tools available. For better controllability of the process, the time is typically in the range of about 1 to 10 minutes, although faster times are possible such as achieved using Rapid Thermal Processing (RTP). In addition, to achieve sufficiently high deposition rates at the relatively low temperatures, the pressure may preferably be greater than about 3 Torr, such as in a range of about 3 to 15 Torr.

**[0020]** At block 50, the tantalum pentoxide layer 33 is annealed, preferably using a remote plasma. The remote plasma produces a high quality tantalum pentoxide layer in terms of low leakage current. The remote plasma may include two separate anneals, wherein a first anneal is in pure nitrogen, and a second is an oxygen and nitrogen anneal, for example, as will be readily appreciated by those skilled in the art. The pressure may be about 1 to 5 Torr during the anneals. Of course, again the temperature is desirably below the oxidation temperature of the metal of the first electrode, such as

below about 500°C, and more preferably below about 400°C.

[0021] Next, the second electrode 34 may be formed over the tantalum pentoxide layer 33 (Block 52). The second electrode 34 may preferably comprise metal, and, more preferably, may preferably comprise any of the metals identified above for the first metal electrode 30. A tungsten plug 35 may be formed to fill the recess defined in the opening by the capacitor layers at Block 45 before stopping (Block 56) as will be readily appreciated by those skilled in the art.

[0022] The method in accordance with the present invention provides a capacitor 20 having a higher capacitance than available in a conventional capacitor including a polysilicon lower electrode, for example. The capacitor 20 produced in accordance with the present invention may have a capacitance value of 20 femtoFarads/cm<sup>2</sup> as compared to a value of half that for a conventional capacitor. The tantalum pentoxide layer 33, because of the remote plasma anneal, has a relatively low leakage current as is also desirable for capacitors in integrated circuit devices as will be understood by those skilled in the art.

#### Claims

1. A method for making an integrated circuit capacitor comprising the steps of:
  - forming a first metal electrode adjacent a semiconductor substrate;
  - forming a tantalum pentoxide layer on the first metal electrode while maintaining a temperature below an oxidizing temperature thereof;
  - performing at least one remote plasma anneal of the tantalum pentoxide layer while maintaining a temperature below the oxidizing temperature of the first metal electrode; and
  - forming a second electrode adjacent the tantalum pentoxide layer after the step of annealing and while maintaining a temperature below the oxidizing temperature of the first metal electrode.
2. A method according to claim 1 wherein the step of forming the tantalum pentoxide layer comprises chemical vapor deposition thereof at a temperature below about 500°C.
3. A method for making an integrated circuit capacitor comprising the steps of:
  - forming a first metal electrode adjacent a semiconductor substrate;
  - forming a tantalum pentoxide layer on the first electrode while maintaining a temperature below about 500°C for a time period of less than about 10 minutes;
- performing at least one remote plasma anneal of the tantalum pentoxide layer while maintaining a temperature below about 500°C; and
- forming a second electrode adjacent the tantalum pentoxide layer after the step of annealing and while maintaining a temperature below about 500°C.
4. A method for making an integrated circuit capacitor comprising the steps of:
  - forming, adjacent a semiconductor substrate, a first metal electrode comprising at least one of titanium, tungsten, tantalum, and alloys thereof;
  - forming a tantalum pentoxide layer on the first metal electrode while maintaining a temperature below about 500°C;
  - remote plasma annealing the tantalum pentoxide layer in a pure nitrogen plasma;
  - remote plasma annealing the tantalum pentoxide layer in a nitrogen and oxygen plasma after the pure nitrogen anneal; and
  - forming a second electrode adjacent the tantalum pentoxide layer after the remote plasma annealing in the nitrogen and oxygen plasma.
5. A method according to any of claims 1, 2 or 4 wherein the step of forming the tantalum pentoxide layer further comprises forming the tantalum pentoxide layer in a time of less than about 10 minutes.
6. A method according to any of claims 1 to 3 wherein the step of forming the first metal electrode comprises forming the first metal electrode to include at least one of titanium, tungsten, tantalum, and alloys thereof.
7. A method according to any of claims 1 to 3 wherein the step of forming the first metal electrode comprises forming the first metal electrode to include at least one of titanium, tungsten, tantalum, platinum, ruthenium, iridium, and alloys thereof.
8. A method according to any of the preceding claims wherein the step of forming the tantalum pentoxide layer comprises chemical vapor deposition thereof at a temperature below about 400°C.
9. A method according to any of the preceding claims wherein the step of forming the tantalum pentoxide layer further comprises forming the tantalum pentoxide layer at a pressure of greater than about 3 Torr.
10. A method according to any of the preceding claims wherein the step of performing at least one remote plasma anneal comprises exposing the tantalum

pentoxide layer to a pure nitrogen containing remote plasma.

11. A method according to claim 10 wherein the step of performing at least one remote plasma anneal comprises exposing the tantalum pentoxide layer to an oxygen and nitrogen containing remote plasma after the pure nitrogen remote plasma anneal. 5
12. A method according to any of the preceding claims wherein the step of forming the second electrode comprises forming a second metal electrode. 10
13. A method according to any of the preceding claims further comprising the steps of: 15
- forming at least one dielectric layer adjacent the semiconductor substrate; and  
forming an opening in the at least one dielectric layer; and 20
- wherein the step of forming the first metal electrode comprises forming the first metal electrode to line the opening in the at least one dielectric layer. 25
14. A method according to any of the preceding claims wherein the step of forming the first metal electrode comprises the steps of forming a first metal layer and nitridizing an upper surface portion thereof. 30
15. A method according to claim 14 wherein the step of nitridizing comprises exposing the first metal layer to a nitrogen containing ambient while maintaining a temperature below the oxidizing temperature of the metal. 35
16. A method according to any of claims 1 to 13 wherein the step of forming the first metal layer electrode comprises depositing a first metal layer and depositing a metal nitride layer thereon while maintaining a temperature below the oxidizing temperature of the metal. 40

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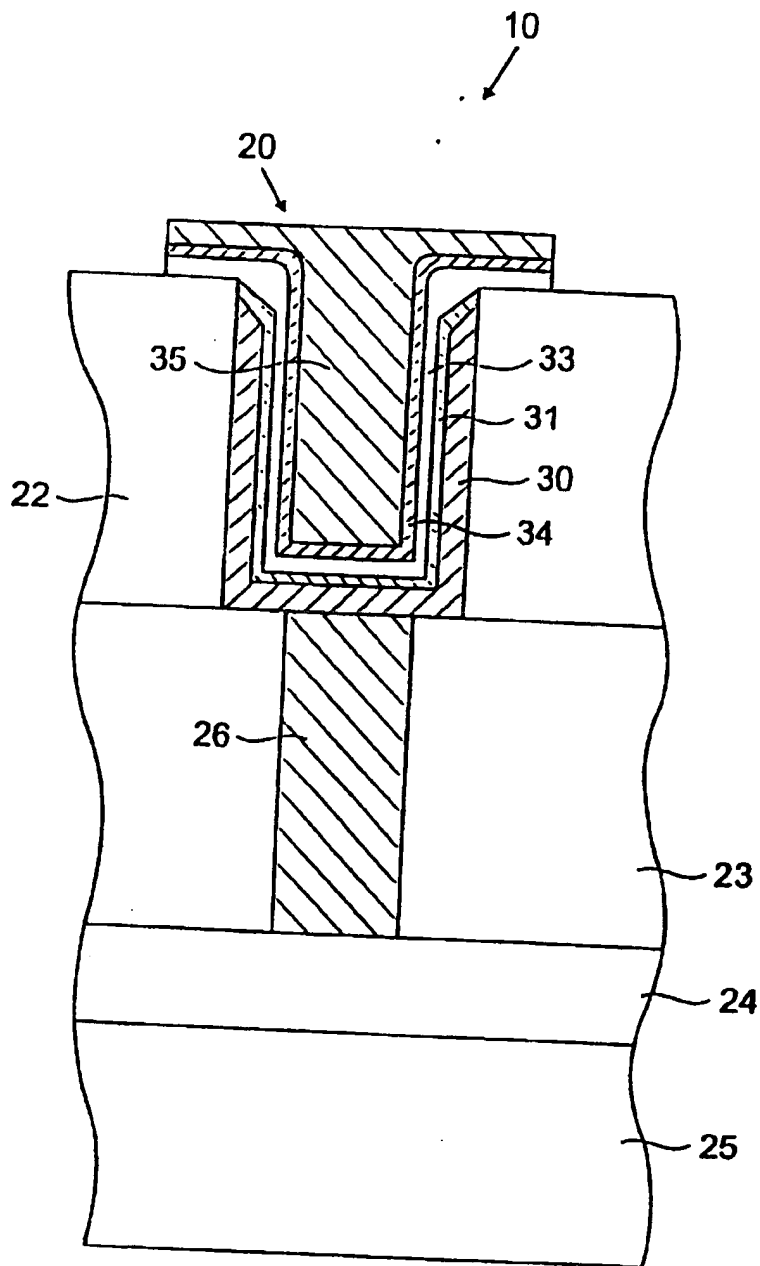


FIG. 1

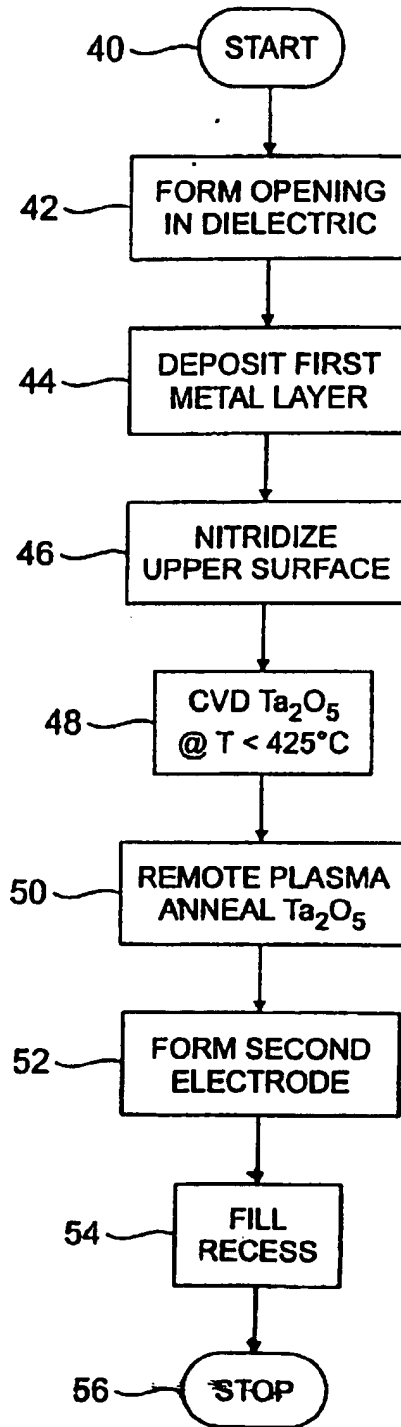


FIG. 2